REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

Claim 19 was rejected under 35 U.S.C. Section 112, first paragraph, as allegedly failing to comply with the written description requirement. While not acquiescing in this rejection, claim 19 has been amended to further recite that one of the unit circuits for the second shift register is disposed in one of the physical spaces. This amendment finds support in Figure 12, for example, and is believed to address the written description issues raised in the office action with respect to claim 19. Consequently, withdrawal of the Section 112, first paragraph, rejection of claim 19 is respectfully requested.

Claims 1-10 and 12-20 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Azami (U.S. Patent No. 6,702,407).

Applicant respectfully traverses this rejection.

Claim 1 recites a shift register block in which *a first circuit, which is not one of a plurality of spaced-apart, cascade-connected unit circuits of a first shift register, is disposed in the physical space between a unit circuit of a preceding output stage and a unit circuit of a following output stage.*

Applicant respectfully submits that Figure 3 of Azami (which is referenced in the office action) is a schematic representation and does not reflect the relative physical arrangement of the various components shown therein. In particular, Azami does not

disclose (or even suggest) how components of a shift register should be physically arranged or laid out relative to one another and to other circuits. Moreover, even assuming it is erroneously argued that Figure 3 shows a physical arrangement, the inverters and NAND gates are not disposed in the physical space between adjacent flip-flops. Consequently, Azami does not disclose the physical arrangement specified in claim 1 and therefore cannot anticipate claim 1 or any of its dependent claims.

As mentioned above, the office action continues to read the schematic diagram of Figure 3 onto the physical arrangement of circuit components recited in the claims. Specifically, the office action contends that "the schematic representation is normally sketched similarly closed (sic: closely) to the physical arrangement." See 9/13/2007 Office Action, page 10. However, the office action provides no documentary evidence in support of the contention regarding the relationship between schematic and physical arrangements in Azami. In any event, Azami's Figure 3 schematic diagram fails to show that the inverter and logic gate are in the space between adjacent flip-flops. Specifically, the inverter and logic gate are positioned beneath the space between adjacent flip-flops.

Claims 8, 9 and 13 also include the above-italicized feature and thus Azami is likewise deficient with respect to these claims and the claims that depend therefrom.

Claim 17 describes unit circuits of a first shift register which are linearly disposed so that physical spaces are provided between each adjacent pair of unit circuits, wherein circuits other than unit circuits of the first shift register are disposed in the physical

spaces between adjacent circuit units. As noted above, Azami does not disclose circuits other than unit circuits disposed in the physical spaces between each adjacent pair of unit circuits as claimed and thus does not anticipate claim 17 or its dependent claims.

Claims 1-10 and 13-20 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Washio et al. (U.S. Patent No. 6,724,361).

Applicant respectfully traverses this rejection.

The office action points to the Figure 11 embodiment showing inverters 24 between the flip-flops of the shift register. Applicants respectfully submit that Figure 11 of Washio is a circuit diagram (see Washio, col. 8, lines 24-25) and does not reflect the relative physical arrangement of the various components shown therein. In particular, Washio does not disclose (or even suggest) how components of a shift register should be physically arranged or laid out relative to one another and to other circuits.

Claim 11 was rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Azami. Applicants traverse the contentions in the office action that the features of claim 11 would have been obvious in view of Azami. In any event, Azami is deficient with respect to the physical layout specified in claim 9, from which claim 11 depends. Consequently, Applicant submits that claim 11 patentably distinguishes from Azami.

Claims 11 and 12 were rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Washio. Applicant traverses the contentions in the office action that

the features of claims 11 and 12 would have been obvious in view of Washio. In any event, Washio is deficient with respect to the physical layout specified in claim 9, from which claims 11 and 12 each depends. Consequently, Applicant submits that claims 11 and 12 patentably distinguish from Washio.

New claims 21-28 have been added. The subject matter of these new claims finds support in the original disclosure and the Examiner is invited to independently confirm that this is the case.

Claims 21-25 respectively depend from claims 1, 8, 9, 13 and 17 and recite that the unit circuits for the first shift register are disposed linearly with the first circuit. This feature finds support in various ones of the example embodiments. See, e.g., Figure 1. These claims distinguish over the applied documents because of their respective dependencies and because these applied documents do not disclose the claimed arrangement of a first circuit and unit circuits.

Claim 26 recites a data signal line driving circuit comprising a first shift register comprising a plurality of cascade-connected first unit circuits for sequentially propagating a first input signal therethrough in response to a first clock signal and a second shift register comprising a plurality of cascade-connected second unit circuits for sequentially propagating a second input signal therethrough in response to a second clock signal. The second unit circuits are linearly aligned with the first unit circuits, and the second unit circuits are disposed in physical spaces between the first unit circuits. The

applied documents do not disclose or suggest first and second shift registers arranged in this manner.

Claims 27 and 28 depend from claim 26. These claims patentably distinguish from the applied documents by virtue of their respective dependencies from claim 26 and by virtue of reciting arrangements of waveform processing circuits not disclosed or suggested by the applied documents.

The pending claims are believed to be allowable and favorable office action is respectfully requested. Should the Examiner feel that further discussion would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,
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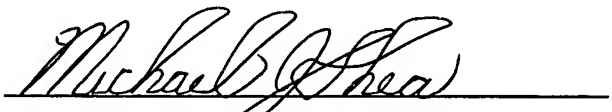
By: 
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